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FAX +49 89 2399 - 4465

Europäisches Patentamt	European Patent Office	Office européen des brevets
Generaldirektion 2	Directorate General 2	Direction Générale 2

Damen, Daniel Martijn
Philips Intellectual Property & Standards
P.O. Box 220
5600 AE Eindhoven
PAYS-BAS

Formalities Officer
Name: Lambert
Tel.: 7574

Date
30.11.06

Reference	Application No./Patent No.
PHNL030726EP2	04744376.7 - 2211
Applicant/Proprietor: Koninklijke Philips Electronics N.V.	

Communication of amended entries concerning the representative (Rule 92(1)h) EPC)

As requested, for the above-mentioned European patent application/European patent the entries concerning the representative have been amended as follows:

Damen, Daniel Martijn
Philips Intellectual Property & Standards
P.O. Box 220
5600 AE Eindhoven
NL

The amendment will be recorded in the Register of European Patents.

Transfer Service
Tel.: +49 (0)89 2399 2780

P.B.5818 - Patentlaan 2
2280 HV Rijswijk (ZH)
(070) 3 40 20 40
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Generaldirektion 1	Directorate General 1	Direction générale 1

de Jong, Durk Jan
Philips
Intellectual Property & Standards
P.O. Box 220
5600 AE Eindhoven
PAYS-BAS

EPO Customer Services
Tel.: +31 (0)70 340 45 00

Date
13-04-2006

Reference	Application No./Patent No.
PHNL030726EP	04744376.7 - 2211 PCT/IB2004050964

Applicant/Proprietor
Koninklijke Philips Electronics N.V.

Communication pursuant to Rules 109 and 110 EPC

(1) Amendment of application documents, especially the claims (R. 109 EPC)

The above mentioned international (Euro-PCT) application has entered the European phase, or can do so, once the necessary conditions are fulfilled.

Under Articles 28, 41 PCT, Rules 52, 78 PCT and Rule 86(2) to (4) EPC, the applicant may amend the application documents after receiving the international search report.

Whether or not he has already done so, he now has a further opportunity to file amended claims or other application documents within a non-extendable time limit of one month after notification of the present communication (R. 109 EPC).

The claims applicable on expiry of the above time limit, i.e. those filed on entry into the European phase or in response to the present communication, will form the basis for the calculation of any claims fee to be paid (see page 2) and for any supplementary search to be carried out under Article 157(2) EPC (R. 109 EPC).

--2/

Registered letter
EPO Form 1226 01.02 EUCL

(2) Claims fees under Rule 110 EPC

If the application documents on which the European grant procedure is to be based comprise more than ten claims, a claims fee shall be payable for the eleventh and each subsequent claim within the period provided for in Rule 107(1) EPC.

☐ Based on the application documents currently on file, all necessary claims fees have already been paid (or the documents do not comprise more than 10 claims).

☑ All necessary fees will be/have been debited automatically according to the automatic debit order.

☐ The claims fees due for the claims ..... to ..... were not paid within the above-mentioned period.

Any non-paid claims fee, either based on the current set of claims or on any amended claims to be filed pursuant to Rule 109 EPC (see page 1), may still be validly paid within a non-extendable period of grace of **one month** after notification of this communication.

If a payment is made for only some of the claims, it must be indicated for which claims it is intended. If a claims fee is not paid in due time, the claim concerned is deemed to be abandoned (R. 110(4) EPC).

If claims fees have already been paid, but on expiry of the above-mentioned time limit there is a new set of claims containing fewer fee-incurring claims than previously, the claims fees in excess of those due under Rule 110(2), 2nd sentence, EPC will be refunded (R. 110(3) EPC).

You are reminded that any supplementary search under Article 157(2) EPC will relate only to the last set of claims applicable on expiry of the above time limit AND will be confined to those fee-incurring claims for which fees have been paid in due time.

The fee for the eleventh and each subsequent claim is EUR 40,00.

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de Jong, Durk Jan
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PAYS-BAS

EPO Customer Services
Tel.: +31 (0)70 340 45 00

Date
12.04.06

Reference	Application No./Patent No.
PHNL030726EP	04744376.7 - 2211 PCT/IB2004050964

Applicant/Proprietor
Koninklijke Philips Electronics N.V.

Notification of European publication number and information on the application of Article 67(3) EPC

The provisional protection under Article 67(1) and (2) EPC in the individual contracting states becomes effective only when the conditions referred to in Article 67(3) EPC have been fulfilled (for further details, see information brochure of the European Patent Office "National Law relating to the EPC" and additional information in the Official Journal of the European Patent Office).

Pursuant to Article 158(1) EPC the publication under Article 21 PCT of an international application for which the European Patent Office is a designated Office takes the place of the publication of a European patent application.

The bibliographic data of the above-mentioned Euro-PCT application will be published on 24.05.06 in Section I.1 of the European Patent Bulletin. The European publication number is 1658559.

In all future communications to the European Patent Office, please quote the application number plus Directorate number.

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Generaldirektion 1	Directorate General 1	Direction générale 1

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EPO Customer Services
Tel.: +31 (0)70 340 45 00

Date
24.03.06

Reference	Application No./Patent No.
PHNL030726EP	04744376.7 - 2211

Applicant/Proprietor
Koninklijke Philips Electronics N.V.

The international search report, or the declaration under Article 17(2)(a) PCT, has been published under Article 21(3) and Rule 48 PCT on 09.03.06. That publication takes the place of the mention of publication of the European search report (Art. 157(1) EPC).

The request for examination must be filed within **six months** from the above date (Art. 94(2) in conjunction with Art. 157(1) EPC). It is not deemed to have been filed until the examination fee has been paid. However, under Article 22 or 39 PCT in conjunction with Article150(2) and Rule 107(1) EPC, the time limit for filing it does not expire before the end of the 31st month from the filing date (or earliest priority date). Payment of the designation fees must also be made within the above-mentioned period (R. 107(1) EPC). The same applies also for the extension fees.

If the request for examination is not filed in due time, and at least one designation fee is not paid, the European patent application is deemed to be withdrawn (Art. 94(3), 79(3) and R. 108(1) EPC).

For more details see the Guide for applicants Part 2: PCT proceedings before the EPO-"Euro-PCT".

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Tel.: +31 (0)70 340 45 00

Date
13-02-2006

Reference	Application No./Patent No.
PHNL030726EP	04744376.7 - 2211 PCT/IB2004050964

Applicant/Proprietor
Koninklijke Philips Electronics N.V.

Communication pursuant to Rules 109 and 110 EPC

(1) Amendment of application documents, especially the claims (R. 109 EPC)

The above mentioned international (Euro-PCT) application has entered the European phase, or can do so, once the necessary conditions are fulfilled.

Under Articles 28, 41 PCT, Rules 52, 78 PCT and Rule 86(2) to (4) EPC, the applicant may amend the application documents after receiving the international search report.

Whether or not he has already done so, he now has a further opportunity to file amended claims or other application documents within a non-extendable time limit of one month after notification of the present communication (R. 109 EPC).

The claims applicable on expiry of the above time limit, i.e. those filed on entry into the European phase or in response to the present communication, will form the basis for the calculation of any claims fee to be paid (see page 2) and for any supplementary search to be carried out under Article 157(2) EPC (R. 109 EPC).

--2/

(2) Claims fees under Rule 110 EPC

If the application documents on which the European grant procedure is to be based comprise more than ten claims, a claims fee shall be payable for the eleventh and each subsequent claim within the period provided for in Rule 107(1) EPC.

☐ Based on the application documents currently on file, all necessary claims fees have already been paid (or the documents do not comprise more than 10 claims).

☑ All necessary fees will be/have been debited automatically according to the automatic debit order.

☐ The claims fees due for the claims ..... to ..... were not paid within the above-mentioned period.

Any non-paid claims fee, either based on the current set of claims or on any amended claims to be filed pursuant to Rule 109 EPC (see page 1), may still be validly paid within a non-extendable period of grace of **one month** after notification of this communication.

If a payment is made for only some of the claims, it must be indicated for which claims it is intended. If a claims fee is not paid in due time, the claim concerned is deemed to be abandoned (R. 110(4) EPC).

If claims fees have already been paid, but on expiry of the above-mentioned time limit there is a new set of claims containing fewer fee-incurring claims than previously, the claims fees in excess of those due under Rule 110(2), 2nd sentence, EPC will be refunded (R. 110(3) EPC).

You are reminded that any supplementary search under Article 157(2) EPC will relate only to the last set of claims applicable on expiry of the above time limit AND will be confined to those fee-incurring claims for which fees have been paid in due time.

The fee for the eleventh and each subsequent claim is EUR 40,00.

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To the European Patent Office

Entry into the European phase (EPO as designated or elected Office)

European application number	
PCT application number	PCT/IB2004/050964
PCT publication number	
Applicant's or representative's reference	PHNL030726EP

1. Applicant

Particulars of the applicant(s) are contained in the international publication or were recorded by the International Bureau subsequent to the international publication.	☑
Changes which have not yet been recorded by the International Bureau are set out here:	☐
Address for correspondence	

2. Representative 1

This is the representative who will be listed in the Register of European Patents and to whom notifications will be made

Name	DE JONG, Durk, J.
Address of place of business	Philips Intellectual Property & Standards P.O. Box 220 NL-5600 AE Eindhoven Netherlands
Telephone	+31 40 2743505
Fax	+31 40 2743489
e-mail	
Any additional representative(s) is/are listed here:	☐

3. Authorisation

An individual authorisation is attached.	☐
A general authorisation has been registered under No:	☐
A general authorisation has been filed, but not yet registered.	☐
The authorisation filed with the EPO as PCT receiving Office expressly includes the European phase.	☐

4. Request for examination

Examination of the application under Art. 94 EPC is hereby requested. The examination fee is being (has been, will be) paid.	☑
Request for examination in an admissible non-EPO language:	☑ Verzocht wordt om onderzoek van de aanvrage als bedoeld in Art. 94.

5. Copies

One or more additional sets of copies of the documents cited in the supplementary European search report are hereby requested. ☐

Number of additional sets of copies

6. Documents intended for proceedings before the EPO

6.1 Proceedings before the EPO as designated Office (PCT I) are to be based on the following documents:

the application documents published by the International Bureau (with all claims, description and drawings), where applicable with amended claims under Art. 19 PCT ☑

unless replaced by the amendments attached. ☐

Where necessary, clarifications should be attached as 'Other Documents'

6.2 Proceedings before the EPO as elected Office (PCT II) are to be based on the following documents:

the documents on which the international preliminary examination report is based, including any annexes ☑

unless replaced by the amendments attached. ☐

Where necessary, clarifications should be attached as 'Other Documents'

If the EPO as International Preliminary Examining Authority has been supplied with test reports, these may be used as the basis of proceedings before the EPO. ☑

7. Translations

Translations in one of the official languages of the EPO (English, French, German) are attached as crossed below:

* *In proceedings before the EPO as designated or elected Office (PCT I + II):*

Translation of the international application (description, claims, any text in the drawings) as originally filed, of the abstract as published and of any indication under Rule 13bis.3 and 13bis.4 PCT regarding biological material ☐

Translation of priority application(s) ☐

It is hereby declared that the international application as originally filed is a complete translation of the previous application (Rule 38(5) EPC) ☐

* *In addition, in proceedings before the EPO as designated Office (PCT I):*

Translation of amended claims and any statement under Art. 19 PCT, if the claims as amended are to form the basis for the proceedings before the EPO (see Section 6). ☐

* *In addition, in proceedings before the EPO as elected office (PCT II):*

Translation of annexes to the international preliminary examination report ☐

8. Biological material

The invention relates to and/or uses biological material deposited under Rule 28 EPC. ☐

The particulars referred to in Rule 28(1)(c) EPC (if not yet known, the depository institution and the identification reference(s) [number, symbols, etc.] of the depositor) are given in the international publication or in the translation submitted under Section 7 on: ☐

page(s) / line(s)

A copy of the receipt(s) of deposit issued by the depositary institution

is attached ☐

will be filed at a later date ☐

A waiver of the right to an undertaking from the requester pursuant to Rule 28(3) EPC is attached. ☐

9. Nucleotide and amino acid sequences

The items required under Rules 5.2 and 13ter PCT and Rule 111(3) EPC have already been furnished to the EPO. ☐

The sequence listing as part of the description is attached in PDF format. ☐

The sequence listing does not include matter that goes beyond the content of the application as filed. ☐

In addition, the sequence listing data is attached in computer-readable form in accordance with WIPO Standard 25. ☐

The sequence listing data in computer-readable form in accordance with WIPO Standard 25 is identical to the sequence listing in PDF format. ☐

10. Designation fees

10.1 It is currently intended to pay seven times the amount of the designation fee. The designation fees for all the EPC contracting states designated in the international application are thereby deemed to have been paid (Art. 2 No. 3 RFees). ☑

AT BE BG CH&LI CY CZ DE DK EE ES FI FR GB GR HU IE IT LU MC NL PL PT RO SE SI SK TR

10.2 The declaration in No. 10.1 does not apply. Instead, it is currently intended to pay fewer than seven designation fees for the following EPC contracting states designated in the international application: ☐

It is requested that no communications under Rule 108(3) EPC be issued in respect of any contracting states not indicated.

10.3 If an automatic debit order has been issued (Section 12), the EPO is authorised, on expiry of the basic period under Rule 107(1)(d) EPC, to debit seven times the amount of the designation fee. If states are indicated in No. 10.2, the EPO will debit designation fees for those states only, unless instructed otherwise before the basic period expires. ☑

11. Extension of the European patent

This application is also considered as being a request for extension to all the non-contracting states to the EPC designated in the international application with which "extension agreements" were in force on the date of filing the international application. However, the extension only takes effect if the prescribed extension fee is paid. ☑

It is currently intended to pay the extension fee for the following states:

12. Automatic debit order ☑

Currency: EUR

The EPO is hereby authorised, under the Arrangements for the automatic debiting procedure, to debit from the deposit account below any fees and costs falling due. For designation fees, see "States".The EPO is also authorised, on expiry of the basic period for paying the extension fees, to debit those fees for each of the "extension states" indicated in "States",

Deposit account number: 28090021
Account holder: Philips International B.V. - IP&S

13. Reimbursements (if any) should be made to the following EPO deposit account: ☑

Number and account holder: 28090021, Philips International B.V. - IP&S

14. Fees

		Factor applied	Fee schedule	Amount to be paid
14-1	002 Search fee	0	690.00	0.00
14-2	015 Claims fee	1	40.00	40.00
14-3	020 Basic national fee for an international application	1	90.00	90.00
14-4	033 Renewal fee for the 3rd year	1	380.00	380.00
	Total:		**EUR**	**510.00**

15. Annotations

16. Signature(s) of applicant(s) or representative

Place: **Eindhoven**
Date: **8 November 2005**
Signed by: **Subject: NL, Philips IP&S, J. van der Veer 1086**
Issuer: , European Patent Office, European Patent Office CA
Capacity: **(Representative)**

For employees (Art. 133(3) EPC) having a general authorisation:
General authorisation No.

Europäisches Patentamt
European Patent Office
Office européen des brevets

Acknowledgement of receipt

We hereby acknowledge receipt of the form for entry into the European phase (EPO as designated or elected Office) as follows:

Submission number	77516	
PCT application number	PCT/IB2004/050964	
Date of receipt	8 November 2005	
Your reference	PHNL030726EP	
Applicant		
Country		
Documents submitted	EPF1200.PDF	application-body.xml
	ep-euro-pct.xml	package-data.xml
Submitted by	CN=J. van der Veer 1086,O=Philips IP&S,C=NL	
Method of submission	Online	
Date and time receipt generated	8 November 2005, 15:44:23	
Digest	FF:40:94:A5:AA:A2:D3:26:DA:EC:30:46:47:4C:FA:3A:23:DE:05:FE	

/European Patent Office/

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PAYS-BAS

EPO Customer Services
Tel.: +31 (0)70 340 45 00

Date
03.11.05

Reference	Application No./Patent No.
	04744376.7 - 2211 PCT/IB2004050964

Applicant/Proprietor
Koninklijke Philips Electronics N.V.

Entry into the European phase before the European Patent Office

These notes describe the procedural steps required for entry into the European phase before the European Patent Office (EPO). You are advised to read them carefully: failure to take the necessary action in time can lead to your application being deemed withdrawn.

1. The above-mentioned international patent application has been given European application No. **04744376.7**.

2. Applicants **without** a residence or their principal place of business in an EPC contracting state may themselves initiate European processing of their international applications, provided they do so before expiry of the 31st month from the priority date (see also point 6 below).

   During the European phase before the EPO as designated or elected Office, however, such applicants must be represented by a professional representative (Arts. 133(2) and 134(1), (7) EPC).

   Procedural acts performed after expiry of the 31st month by a professional representative who acted during the international phase but is not authorised to act before the EPO have no legal effect and therefore lead to loss of rights.

   Please note that a professional representative authorised to act before the EPO and who acted for the applicant during the international phase does not automatically become the representative for the European phase. Applicants are therefore strongly advised to appoint in good time any representative they wish to initiate the European phase for them; otherwise, the EPO has to send all communications direct to the applicant.

3. Applicants **with** a residence or their principal place of business in an EPC contracting state are not obliged to appoint, for the European phase before the EPO as designated or elected Office, a professional representative authorised to act before the EPO.
   However, in view of the complexity of the procedure it is recommended that they do so.

4. Applicants and professional representatives are also strongly advised to initiate the European phase using EPO Form 1200 (available free of charge from the EPO). This however is not compulsory.

5. **To enter the European phase before the EPO**, the following acts must be performed.
(N.B.: Failure validly to do so will entail loss of rights or other adverse legal consequences.)

5.1 If the EPO is acting as **designated** or **elected** Office (Arts. 22(1)(3) and 39(1) PCT respectively), applicants must, within 31 months from the date of filing or (where applicable) the earliest priority date:

a) Supply a translation of the international application into an EPO official language, if the International Bureau did not publish the application in such a language (Art. 22(1) PCT and Rule 107(1)(a) EPC).
If the translation is not filed in time, the international application is deemed withdrawn before the EPO (Rule 108(1) EPC).
This loss of rights is deemed not to have occurred if the translation is then filed within a two-month grace period as from notification of an EPO communication, provided a surcharge is paid at the same time (Rule 108(3) EPC).

b) Pay the national basic fee (EUR 160,00) and, where a supplementary European search report has to be drawn up, the search fee (EUR 960,00 ; Rule 107(1)(c) and (e) EPC).

c) If the time limit under Article 79(2) EPC expires before the 31-month time limit, pay the designation fee (EUR 75,00) for each contracting state designated (Rule 107(1)(d) EPC).

d) If the time limit under Article 94(2) EPC expires before the 31-month time limit, file the written request for examination **and** pay the examination fee (EUR 1430,00 ; Rule 107(1)(f) EPC).

e) Pay the third-year renewal fee (EUR 380,00) if it falls due before expiry of the 31-month time limit (Rule 107(1)(g) EPC).

If the fees under (b) to (d) above are not paid in time, or the written request for examination is not filed in time, the international application is deemed withdrawn before the EPO, or the contracting-state designation(s) in question is (are) deemed withdrawn (Rule 108(1) and (2) EPC). However, the fees may still be validly paid within a two-month grace period as from notification of an EPO communication, provided the necessary surcharges are paid at the same time (Rule 108(3) EPC). For the renewal fee under (e) above, the grace period is **six** months from the fee's due date (Article 86(2) EPC).

5.2 If the application documents on which the European grant procedure is to be based comprise more then ten claims, a claims fee is payable within the 31-month time limit under Rule 107(1) EPC for the eleventh and each subsequent claim (Rule 110(1) EPC). The fee can however still be paid within a one-month grace period as from notification of an EPO communication pointing out the failure to pay (Rule 110(2) EPC).

6. If the applicant had a representative during the application's international phase, the present notes will be sent to the representative, asking him to inform the applicant accordingly.

All subsequent communications will be sent to the applicant, or - if the EPO is informed of his appointment in time - to the applicant's European representative.

7. For more details about time limits and procedural acts before the EPO as designated and elected Office, see the EPO brochure

   How to get a European patent
   Guide for applicants - Part 2
   PCT procedure before the EPO - "Euro-PCT"

   This brochure, the list of professional representatives before the EPO, Form 1200 and details of the latest fees are now all available on the Internet under

   http://www.european-patent-office.org

RECEIVING SECTION

NL 0307726

IB/2004/050264

Europäisches Patentamt
European Patent Office
Office européen des brevets

Bescheinigung Certificate Attestation

Die angehefteten Unterlagen stimmen mit der ursprünglich eingereichten Fassung der auf dem nächsten Blatt bezeichneten europäischen Patentanmeldung überein.

The attached documents are exact copies of the European patent application described on the following page, as originally filed.

Les documents fixés à cette attestation sont conformes à la version initialement déposée de la demande de brevet européen spécifiée à la page suivante.

Patentanmeldung Nr. Patent application No. Demande de brevet n°

03101877.3 ✓

PRIORITY DOCUMENT
SUBMITTED OR TRANSMITTED IN COMPLIANCE WITH RULE 17.1(a) OR (b)

Der Präsident des Europäischen Patentamts;
Im Auftrag

For the President of the European Patent Office

Le Président de l'Office européen des brevets
p.o.

R C van Dijk

Anmeldung Nr:
Application no.: 03101877.3
Demande no:

Anmeldetag:
Date of filing: 25.06.03
Date de dépôt:

Anmelder/Applicant(s)/Demandeur(s):

Koninklijke Philips Electronics N.V.
Groenewoudseweg 1
5621 BA Eindhoven
PAYS-BAS

Bezeichnung der Erfindung/Title of the invention/Titre de l'invention:
(Falls die Bezeichnung der Erfindung nicht angegeben ist, siehe Beschreibung.
If no title is shown please refer to the description.
Si aucun titre n'est indiqué se referer à la description.)

INSTRUCTION CONTROLLED DATA PROCESSING DEVICE

In Anspruch genommene Priorität(en) / Priority(ies) claimed /Priorité(s) revendiquée(s)
Staat/Tag/Aktenzeichen/State/Date/File no./Pays/Date/Numéro de dépôt:

Internationale Patentklassifikation/International Patent Classification/
Classification internationale des brevets:

G06F9/00

Am Anmeldetag benannte Vertragstaaten/Contracting states designated at date of filing/Etats contractants désignées lors du dépôt:

AT BE BG CH CY CZ DE DK EE ES FI FR GB GR HU IE IT LU MC NL
PT RO SE SI SK TR LI

Instruction controlled data processing device

The invention relates to an instruction controlled data processing device.

PCT patent application No. WO00/60457 discloses a VLIW processing device. A VLIW processing device contains a plurality of functional units that are each capable of executing an instruction in parallel with other functional units. A VLIW processing device processes VLIW instruction words that each generally contain a plurality of instructions for execution in parallel by respective functional units. A VLIW processor has the advantage of enabling high-speed execution of programmed processing tasks, but this advantage is bought at the expense of high memory use and high power consumption. WO00/60457 aims to reduce the instruction memory size needed for programs for VLIW processing devices. For this purpose the processing device composes VLIW instructions in response to instructions in a memory. Thus, an original instruction from memory is translated into a plurality of instructions in a VLIW instruction word, to be executed in parallel with different functional units.

High power consumption is caused, among others, by the need to issue many instructions in parallel and the need to access a register file for each issued instruction. These problems are not addressed by WO00/60457.

Among others, it is an object of the invention to provide for a reduction of power consumption in an instruction controlled processing device.

Among others, it is an object of the invention to provide for a reduction of power consumption in particular in a VLIW processing device.

The device according to the invention is set forth in Claim 1. This device contains a group of functional units that are connected in parallel to an issue slot and ports of a register file, for alternatively executing instructions issued from the issue slot with operands from at least one port and writing results to at least one port. In addition to these alternative instructions, the device provides for a combination instruction in response to which more than one functional unit from the group responds, a result from a first one of the functional units being routed to an operand input of a second one of the functional units in response to the combination instruction. The result of the second one of the functional units is used to produce the result of the combination instruction. By using a combination instruction, one

can reduce the number of instructions that needs to be issued to the group of functional units during execution of a program for a give task, thereby reducing power consumption. In contrast to WO00/60457, the combination instruction is not split out into multiple instructions that have to be issued separately, but issued in one issue slot. Thus, the device partly goes against the philosophy of VLIW processing, by partly avoiding the need to issue instructions for different functional units in parallel, even though, of course, other instructions may be issued in parallel with the combination instruction in a same VLIW instruction word.

In an embodiment the processing device has a selectable clock rate for instruction cycles. By reducing the clock rate used during execution of processing tasks that do not need a higher clock rate, power consumption is reduced. When a processing task has to be executed at high speed the clock rate is increased up to a maximum at which all individual functional units can just execute the instruction within one instruction cycle. According to one aspect of the invention the device is constructed so that more than one functional unit responds to the combination instruction in the same instruction cycle, acting in series, and the clock rate can be increased to such a high speed that the series execution of the combination instruction no longer fits within one instruction cycle. When the clock rate is increased to such a level, use of the combination instruction is avoided, for example by executing only programs that do not contain combination instructions, or switching between alternative versions of program that do and do not use combination instructions to accomplish the same task respectively, or by translating the combination instructions into instructions executed by different functional units in successive cycles.

In this way, increased power saving can be realized, because when the device executes at a slow clock rate the total number of instructions that has to be issued to execute a processing task can be reduced by combining instructions into a combination instruction, for which the issue slot needs to be active only during one instruction cycle. When the combination instruction does not use up more instruction cycles than normal instructions its use reduces the time needed to execute a program, making it possible to reduce the clock rate even further for a processing task that has to be executed in a specified time interval.

In another embodiment the processing device is a VLIW processor that contains a plurality of functional units to which instructions from an instruction word can be issued in parallel, for execution in parallel. In this embodiment a bypass coupling is provided from a result output of a further functional unit, which receives an instruction in parallel with the group of functional units that receives the combination instruction, to an operand input of

the second one of the functional units that responds to the combination instruction and also receives the result of the first one of the functional unit. Preferably, the bypass connection contains no latch for pipelining the execution stage executed by the functional units over multiple instruction cycles. Thus, a VLIW instruction word may be used that contains a combination instruction for one group together with another instruction for a functional unit that delivers an operand used during execution of the combination instruction. As a result at sufficiently low clock speeds fewer instructions need to be issued, while still maintaining sufficient speed.

In a further embodiment execution of the combination instruction may extend over more than one instruction cycle. Thus, the combination instruction can also be executed at clock rates at which series execution does not fit within one instruction cycle. In one embodiment intermediate registers are provided to latch results that are routed from one functional unit to another when both functional units respond to the combination instruction. However, this requires additional power consumption by the register and it splits execution. In another embodiment no register is used between the functional units, making use of wave pipelining to pass results from one functional unit to another in part of an interval that spans more than one instruction cycle.

These and other objects and advantageous aspects of the invention will be described using the following figures

Figure 1 shows a processing device

Figure 2 shows a group of functional units

Figures 3a,b show timing aspects

Figure 4 shows a plurality of groups of functional units

Figure 5 shows a further group of functional units

Figure 1 shows a processing device comprising an instruction memory 17, an instruction issue unit 10, with an issue slot 11, a group of functional units 12, a register file 14, a clock circuit 16, a clock rate selection circuit 18 and a program counter 19. Program counter 19 has an output coupled to an address input of instruction memory 17. Instruction memory 17 has an output coupled to instruction issue unit 10. Issue slot 11 of instruction issue unit 10 contains outputs for an operation code coupled to group of functional units 12

and a first operand register address and a second operand register address and a result register address coupled to register file 14. Group of functional units 12 has operand inputs coupled to outputs of register file 14 and a result output coupled to an input of register file 14.

Although only one group of functional units 12 is shown, it should be understood that a plurality of groups may be present in parallel. In this case instruction issue unit contains a respective issue slot for each group of functional units, with an output coupled to an operation code input of the relevant group and register address outputs coupled to register file 14. Also in this case register file 14 has a separate result input for each group of functional units, as well as a separate operand output.

Clock rate selection circuit 18 has an output coupled to a control input of clock circuit 16 and program counter 19. Clock circuit 16 has a clock output coupled to instruction issue unit 10 and register file 14. Instruction issue unit 10 is coupled to program counter 19. In operation a clock signal from clock circuit 16 defines successive instruction cycles. Normally a respective instruction is executed in each instruction cycle. In each instruction cycle instruction issue unit 10 issues an operation code of a command that is part of an instruction to group of functional units 12. Similarly, instruction issue unit 10 issues operand register addresses for an instruction to register file 14 in each instruction cycle and instruction issue unit 10 issues a result register address for an instruction to register file 14 in each instruction cycle. Due to pipelining, the operation code, operand register addresses and result register address that are issued in the same instruction cycle may belong to different instructions.

In an instruction cycle group of functional units 12 executes a command identified by the operation code from instruction issue unit 10, using one or more operands received from register file 14.

Figure 2 shows group of functional units 12 in more detail. Group 12 contains a plurality of functional units 20a,b (only two shown for the sake of clarity, but more may be present). Operand inputs 22a,b of group 12 are coupled to operand inputs of functional units 20a,b. Result outputs of functional units 20a,b are coupled to a result output of group 12 via an output multiplexer 26. An operation code input 24 is coupled to operation code inputs of functional units 20a,b and output multiplexer 26 (preferably operation code 24 is coupled to functional units 20a,b and output multiplexer 26 via a pre-decoder, but this is not shown for the sake of clarity).

Group 12 also contains a control unit 28 and an input multiplexer 29. Input multiplexer 29 has a first input coupled to operand input 22a of the group and an output

coupled to an operand input of a second functional unit 20b. A second input of input multiplexer 29 is coupled to a result output of a first functional unit 20a. Control unit 28 is coupled to operation code input 24 and has an output coupled to a selection input of input multiplexer 29.

In operation, received operation codes of a first type each identify one of the functional units 20a,b which executes the operation code. For operation codes of this first type control unit 28 makes input multiplexer 29 pass the operand from operand input 22b. The identified functional unit 20a,b executes a processing operation (for example ADD, or Multiply) identified by the operation code, using the operands applied to its operand inputs. The identified functional unit 20a,b outputs a result. Output multiplexer 26 passes the result from the identified functional unit 20a,b to the result output of the group of functional units 12.

Figure 3a shows timing aspects of execution of operations by functional units 20a,b. On top a trace 30 indicates successive instruction cycles. Each instruction cycle lasts for a duration of T1. Below the top line minimum time intervals 32, 34 have been indicated that are needed by functional units 20a,b to produce results during execution. Time intervals 32, 34 may depend on the kind of operation that is selected by the operation code, on the functional unit 20a,b that executes the operation and the operand data used in the operation. However, the result is always available before the end of the instruction cycle, i.e. the duration of the intervals is shorter than T1. It should be noted that figure 3a only shows intervals needed for execution in a functional unit. In practice, operation may be pipelined, so that processing of each instruction involves an instruction fetch stage, an operand fetch stage, an execution stage and a result write stage, the different stages being executed in successive instruction cycles, if need be after latching intermediate results. Time intervals 32, 34 concern only the execution stage.

The operation codes also include operation codes of a second type, which result in operation of a cascade of functional units 20a,b. When an operation code of the second type is applied to operand input 24, control unit makes input multiplexer 29 pass a result from a first one of the functional units 20a to an operand input of a second one of the functional units 20b. Output multiplexer 26 passes the result from second one of the functional units 20b to the result output of group of functional units 12.

As an example of an operation code of the second type is an operation code for the computation of an operand to a sum of a square

result = A*A+B

In this example, first functional unit 20a of group 12 is a multiplier and second functional unit 20b of group 12 is an adder. The operation has the register addresses of registers that contain A and B as operands. In response to the operation code first functional unit 20a of group 12 forms the product A*A. In response to the same operation code control unit 28 causes multiplexer 29 to pass the products A*A as operand to second functional unit 20b of group 12. Still in response to the same operation code second functional unit 20b of group 12 forms a sum A*A+B of the received products A*A and the operand B. It should be appreciated that this operation code is merely an example. Operation codes may be provided for other operations (e.g. A*A-B, A/((A+B), etc. A*B+A), a single such operation code may be supported or a plurality.

When more operands are available either through inclusion of more than two operand register addresses in a command, or through inclusion of more than one operand in the same register, more complicated operations may be executed. E.g. when operands contain pairs of numbers (ReA,ImA) and (ReB, ImB) that each represent the real part and the imaginary part of a complex number, a combination operation may instruct multiplier functional units to form products of the real parts (ReA*ReB) and of the imaginary parts (ImA*ImB) respectively and an adder to sum the products. In this case, group 12 preferably contains at least two multipliers and an adder as functional units, as well as multiplexers under control of control unit 28 to select whether the adder receives operands from operand inputs 22a,b or from the multipliers.

Figure 3b shows timing aspects of the execution stage of execution of an operation selected by an operation code of the second type. In this case, the duration of instruction cycles is T2. The duration of time interval 36 needed before a result of this operation is available is a sum of a duration of a first time interval 36a needed by the first one of the functional units 20a, a duration of a second time interval 36b needed to pass the result of the first one of the functional units 20a to the operand input of the second one of the functional units 20b and a duration of a third time interval 36c needed by the second one of the functional units 20b (To be more precise, instead of the duration of second time interval 36b one should consider a difference between the duration of the time interval needed to pass the result from the output of the first one of the functional units 20a to the operand input of the second one of the functional units 20b minus the duration of the interval needed to pass an external operand to this operand input; this difference may be negative).

The overall duration of the interval 36 before the result of an operation of the second type is available is longer than the duration of the intervals 36a, 36c needed by the functional units 20a,b for the operations of which the operation is made up. Nevertheless this overall duration should fit within the duration T2 of an instruction cycle.

Clock rate selection circuit 18 supplies a signal to clock circuit 16 to select the clock rate, i.e. the duration T1 or T2 of the instruction cycle. Preferably, the clock rate is set as low as possible (to an instruction cycle duration that is as long as possible) without compromising the ability to executed of required tasks within a required time-interval. By reducing the clock rate power consumption of the device is reduced.

The selectable clock rates include a slow clock rate at which the duration execution of instructions of the second type fits within an instruction cycle (duration T2) and a fast clock rate at which the duration execution of instructions of the second type does not fit within an instruction cycle (duration T1). When the clock rate is set at the slow clock rate a task is executed using instructions with operation codes of the second type. When the clock rate is set at the fast clock rate the task is executed without using instructions with operation codes of the second type, e.g. by replacing each instruction with an operation code of the second type by more than one instruction with an operation code of the first type. By using instructions with operation codes of the second type at the slow clock rate the number of instruction cycles needed to execute a task is reduced. Thereby execution speed is increased.

Any way of adapting the instructions employed in executing the task may be used. In one embodiment, instruction memory 17 stores instructions of at least two programs for executing the same task, one using instructions with operation codes of the first type and another one not using such instructions. In this embodiment clock rate selection circuit 18 selects the relevant program in addition to the clock rate, for example by setting the initial value of program counter 19 at the start of execution of the task.

However, many other ways may be used to avoid the use of operation codes of the second type during execution of the task. For example, instructions may be executed to jump to either a program with operation codes of the second type or without this type of operation codes, dependent on the clock rate that has been set. Similarly, translation of instruction addresses into physical memory addresses may be made dependent on the selected clock rate so as to select the appropriate instructions. In these cases it is not necessary to provide alternative versions (with and without operation codes of the second type) of the whole program for executing a task: instead alternative versions may be provided only for sections of the program that contain such instructions (in this case instructions with operation

codes of the second type are preferably included only in frequently executed sections). As an alternative instruction issue unit may even be arranged to translate an instruction with an operation code of the second type into a plurality of instructions without such operation codes on the fly, if the fast clock rate has been selected.

Preferably the operation codes of the second type support frequently executed instructions.

Although the invention has been illustrated by means of an embodiment with a clock rate selection circuit 18, it will be understood that the clock rate may be selected in other ways, for example under control of the part of the program counter value, so that the clock rate is set dependent on the segment of a program from which instructions are being executed, or under control of instructions from the program.

Figure 2 illustrates an embodiment in which several functional units 20a,b respond to the same operation code of the second type. In addition control unit 28 responds to this operation code and output multiplexer 26 outputs a result from only one of the responding functional units 20a,b. However, it will be understood that a (pre-)decoder (not shown) may used that detects which functional units must be activated in response to an operation code and that activates these functional units 20a,b. In this case the (pre-)decoder activates one functional unit 20a,b per instruction cycle when the operation code is of the first type and a combination of functional units when the operation code is of the second type. As shown, each of the functional units 20a,b that is activated in response to the operation code of the second type is also able to respond individually to an operation code of the first type. Thus, instruction units 20a,b are efficiently reused. However, in an alternative, a part of the functional units 20a,b that is used to execute an operation code of the second type in cascade may be of a type that does not respond individually to any operation code of the first type. Thus a certain overhead has to be introduced into the group of functional units 12.

Although only a single input multiplexer 29 is shown by way of example, and only two functional units 20a,b, it will be understood that in practice more complicated connection networks may be provided between the outputs of functional units 20a,b or additional function units (not shown) in group 12.

Figure 4 shows two groups 12, 40 of functional units for use in a processing device as shown in figure 1, implementing a further aspect of the invention. Each of the groups 12, 40 has an operation selection input 24, 48 coupled to a respective issue slot from the instruction issue unit (not shown), and to read and write ports of the register file (not shown). Thus, the device is a VLIW processor (Very Long Instruction Word processor) that

contains multiple, substantially independently selectable commands for different groups 12, 40. A first one of the groups 12 is arranged as shown in figure 2, except that a further multiplexer 44 has been added, to a first input of which the second operand input 22b of group 12 is coupled. An output of further multiplexer 44 is coupled to an operand input of second functional unit 20b. Further multiplexer 44 has a control input coupled to control unit 28.

A second group of functional units 40 contains a number of functional units 40a, 40b. The output of one of the functional units 40b of second group 40 is coupled to a second input of further multiplexer 44 via a bypass connection 42.

In operation control unit 28 recognizes when the operation code of a combination instruction is issued to group of functional units 12. If so, control unit 28 causes multiplexers 29, 44 to pass operands from the first functional unit 20a of group 12 and from functional unit 40b of further group 40 to the operand inputs of second functional unit 20b of group 12. Both first and second functional unit 20a,b of group 12 respond to the combination instruction, first functional unit 20a receiving operands from the operand inputs 22a,b of group 12, multiplexer 26 passing the result from second functional unit 20b to the write port of register file that is provided for group 12.

A program stored in instruction memory 17 contains an instruction that contains commands for both groups 12, 40. The instruction contains a combination command for a first group 12 and the command for the second group 40 contains an operation code that activates second functional unit 40b of the second group. Thus, in response to the instruction, both first functional unit 20a of first group 12 and second functional unit 40b of second group 40 produce results that are used as operands by second functional unit 20b of group 12. The result from second functional unit 40b of second group 40 is passed between the groups 12, 40 via bypass connection 42. Multiplexers 29, 44 pass the results as operands to second functional unit 20b of first group 12.

As an example, this type of instruction may be used for a multiply-add operation in which the products of two pairs of operands are added

result = A*B+C*D

In this example, first functional unit 20a of first group 12 is a multiplier, second functional unit 40b of second group 40 is a multiplier and a second functional unit 20b of first group 12 is an adder. The instruction contains a multiply-add command (the combination command)

that is issued to first group 12 and a multiply command that is issued to second group 40. The multiply-add command has the register addresses of registers that contain A and B as operands and the multiply command has the addresses of registers that contain C and D as operands. In response to the instruction first functional unit 20a of first group 12 and second functional unit 40b of second group 40 form the product A*B and C*D respectively. In response to the same multiply-add instruction control unit 28 causes multiplexers 29, 44 to pass these products as operands to second functional unit 20b of first group 12. Still in response to the same multiply-add instruction second functional unit 20b of first group 12 forms a sum A*B+C*D of the received products A*B and C*D.

This type of combined multiplication and addition is a frequently occurring combination of instructions, for example in multiplication of complex numbers and therefore the instruction realizes considerable savings in the number of instructions that need to be issued for this type of operation. However, it should be realized that the invention is not limited to this instruction. For example, a similar technique could be applied to multiplication and subtraction, to compute A*B-C*D, or to any other combination of operations that occurs in certain program. The device may support an operation code for one combination instruction only or for a plurality of such instructions.

It should be noted that, when executing a program with the functional units of the embodiment of figure 4, when the instruction cycle rate is too fast to accommodate the delays of second functional unit 40b of second group 40 and second functional unit 20b of first group 12 in succession, the program may be adapted so as to eliminate combination instructions, as discussed in the context of figure 2. The combination instruction may provide for selection of results from different functional units (alternative to second functional unit 40b of second group 40) for use as operand for second functional unit 20b of first group 12. These different functional units may be part of a single group 40 or of a plurality of different groups. Without deviating from the invention second group 40 may contain only one functional unit (second functional unit 40b).

Figure 5 shows an alternative group of functional units 12 for use in the device. In the embodiments show this far, the combination operation is executed in a single instruction cycle. In the embodiment of figure 5 multiple instruction cycles are used. Group of functional units 12 contains a control register 50 with an input coupled to control unit 28 and outputs coupled to control inputs of multiplexers 29, 44 and second functional unit 20b. First data inputs of multiplexers 29, 44 are connected to operand inputs 22a,b. Result registers 52, 54 are provided with outputs coupled to second data inputs of multiplexers 29,

44. Inputs of result registers 52, 54 are coupled to the result outputs of one or more functional units (e.g. 20a) in group 12 and/or to the result outputs of one or more functional in other groups (not shown). The input connections are not shown for the sake of clarity.

In operation, control unit 28 responds to a combination instruction issued for execution in a first instruction cycle by causing control register 50 to load information for controlling multiplexers 29, 44 and second functional unit 20b of first group 12. This information controls multiplexers 29, 44 and second functional unit 20b of first group 12 in a second instruction cycle that follows the first instruction cycle. In the second instruction cycle results latched in result registers 52, 54 are passed as operands to second functional unit 20b of group 12 and this second functional unit 20b receives a control signal to execute its part of the command implied by the combination instruction in the second instruction cycle. In response second functional unit 20b produces a result at the end of the second instruction cycle.

In this way a next instruction can be executed in group 12 in the second instruction cycle, in parallel with execution of part of the combination instruction by second functional unit 20b. For example, execution of a first instruction to compute A*B-C*D could be started in a first instruction cycle and a second instruction to compute A*D+B*C could be started in the next instruction cycle. Thus, the real and imaginary parts of two numbers A+iC and B+iD are computed using two instructions.

Of course it should be avoided that a conflict occurs between the results from both the combination instruction and the next instruction. This may be realized in various ways. In one embodiment the next instruction is selected from a subset of instructions that do not produce a result in the second instruction cycle (e.g. another combination instruction, or a NOP instruction). In this embodiment control register 50 also controls output multiplexer 26 to pass the result from second functional unit 20b. In another embodiment a bypass register (not shown) may be used to pass the result of second functional unit 20b in parallel with the result from the functional unit that responds to the next instruction.

It should be noted that in the embodiment of figure 5 the program need not be adapted when the instruction cycle rate is too fast to accommodate the delays of the first and second functional unit 20a,b in a single instruction cycle.

Although figure 5 shows result registers 52, 54 inserted before multiplexers 29, 44, these registers 52, 54 may be omitted if wave pipelining is used. In this case propagation delays within the functional units 20a,b are used to allow results from the combination instruction and the next instruction to be present simultaneously at the outputs

of second functional unit 20b and the functional unit that executes the next instruction. In a further embodiment registers may be provided in front of the particular functional units that produce the results used by second functional unit 20b of first group 12. These registers are arranged to respond to the combination instruction by latch the operands of these functional units and to supply these operands, after the operands have been applied directly from inputs 22a,b in a first instruction cycle, to the particular functional units also during a subsequent instruction cycle.

Although the invention has been illustrated using combination instructions involving successive execution of two functional units in series in response to the same command, it will be understood that combination commands may be provided involving a greater number of functional units in series.

CLAIMS:

1. An instruction controlled data processing device, the device comprising

- an instruction issue unit (10), having an issue slot (11) for issuing instructions from an instruction set, the instruction issue unit issuing respective ones of the instructions in successive instruction cycles;
- a register file (14) with an read port and a write port;
- a group (12) of functional units (20a,b), each functional unit (20a,b) having a control input coupled to the issue slot (11), an operand input (22a,b) coupled to the read port and a result output coupled to the write port, each functional unit (20a,b) being arranged to respond to instructions from a respective sub-set of the instruction set to which the other functional units (20a,b) do not respond, the instruction set further comprising a combination instruction to which a first and second one of the functional units (20a,b) respond;
- a control unit (28) coupled to the issue slot (11) and responsive to the combination instruction from the instruction set, to route the result output of the first one of the functional units (20a) to the operand input of the second one of the functional units (20b).

2. An instruction controlled data processing device according to Claim 1, organized as a VLIW processor, the issue slot (11) being one of a plurality of issue slots of the instruction issue unit for issuing a VLIW instruction word that contains the combination instruction as one of its instructions, the register file (14) having a plurality of sets of read and write ports, the device comprising respective functional units or groups of functional units each coupled to a respective one of the issue slots and the sets of read and write ports for executing respective instructions from the VLIW instruction word, the first and second one of the functional units in responding to the combination instruction issued in the issue slot in parallel with execution of instructions issued in the same instruction word as the combination instruction.

3. An instruction controlled data processing device according to Claim 1, wherein the first and second one of the functional units (20a,b) respond to the combination instruction in a same instruction execution cycle.

4. An instruction controlled data processing device according to Claim 3 , comprising a clock circuit (16) for clocking the instruction cycles, the clock circuit (16) having a plurality of selectable clock rates, including a first clock rate that is sufficiently slow to accommodate within an instruction execution cycle the latency involved in producing a result from the second one of the functional units (20b) in response to an operand applied to the first one of the functional units (20a) also during execution of the combination instruction within the instruction execution cycle, and a second clock rate that is too fast to accommodate said latency in the instruction cycle, but accommodates latency of instructions from said sub-sets.

5. An instruction controlled data processing device according to Claim 1, wherein the instruction issue unit (10) has a further issue slot and the register file (14) has a further read port, the device comprising a further functional unit (40b) having a control input coupled to the further issue slot and an operand input coupled to the further read port, the control unit (28) being arranged to route the result output of the further functional units (40b) to a further operand input of the second one of the functional units (20b) under control of the combination instruction, bypassing the register file (14) under control of the combination instruction.

6. An instruction controlled data processing device according to Claim 5, programmed with a program that contains a VLIW instruction that contains a command for the further functional unit (40b) and the combination instruction for the group of functional units (12) for issue in a same instruction cycle.

7. An instruction controlled data processing device according to Claim 1, wherein the control unit (28) is arranged to make the second one of the functional units (20b) respond to the combination instruction in an instruction execution cycle following an instruction execution cycle in which the first one of the functional units (20a) responds to the combination instruction.

8. An instruction controlled data processing device according to Claim 7, wherein the result of the first one of the functional units (20a) is routed without intermediate

latching from the first one of the functional units (20a) to the operand input of the second one of the functional units (20b).

9. A method of executing a processing task, the method comprising

- providing a group of functional units (12),
- issuing successive instructions to the group (12);
- executing those of the instructions that are of a first type each with an individual one of the functional units (20a,b),
- executing an instructions that is of a second type with a first and a second one of the functional units in series (20a,b);
- routing a result of the first one of the functional units (20a) to an operand of the second one of the functional units (20b) in response to the instruction of the second type.

10. A method according to Claim 9, wherein the first and the second one of the functional units (20a,b) respond to the instruction of the second type in a same instruction execution cycle, the method comprising

- selecting an instruction cycle rate from at least a first and second rate, the first rate being so slow that execution of a combination instruction by a cascade of at least two of the functional units (20a,b) fits within an instruction cycle at the first rate, the second rate being so fast that only execution of instructions by single ones of the functional units fits within the instruction execution cycle at the second rate, execution of the combination instruction not fitting within one instruction execution cycle at the second rate;
- adapting the instructions used to execute the processing task to the selected instruction cycle rate, so that the combination instruction is used when the task is executed at the first rate and the combination instruction is replaced by instructions of the first type with corresponding effect when the task is executed at the second rate.

11. A method according to Claim 9, comprising

- issuing the successive instructions each as part of a VLIW instruction word that contains a plurality of instructions for respective further functional units (40a,b);
- including in the instruction word that contains the instruction of the second type an further instruction for a particular one of the further functional units (40a,b);

- routing a further result of the further instruction from the particular one of the further functional units (40a,b) to a further operand input of the second one of the functional units (20b) in response to the instruction of the second type.

ABSTRACT:

The data processing device has a plurality of functional units and issues instructions in successive instruction cycles. Instructions of a first type are each intended for one functional unit at a time. An instruction of a second type causes a combination of functional units to respond in the same instruction execution cycle, a result from one functional unit being used by another as part of the execution of the same instruction. Preferably, the device supports alternative operation at a number of different instruction cycle rates, dependent on whether an executed program segment contains instructions of the second type. The fastest instruction cycle rate does not allow execution of the instruction of the second type, because operation by different functional units does not fit within the instruction execution cycle. When possible, the device saves power by switching to a slower clock rate, in which case instructions of the second type are executed to save additional power, by reducing the number of instructions that have to be issued.

Fig. 1

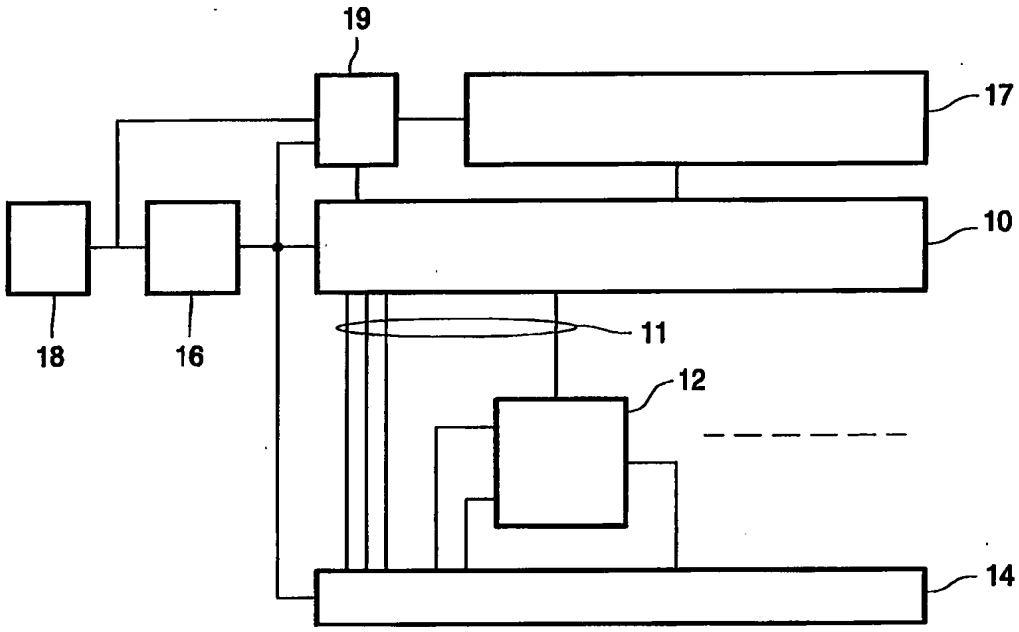

FIG. 1

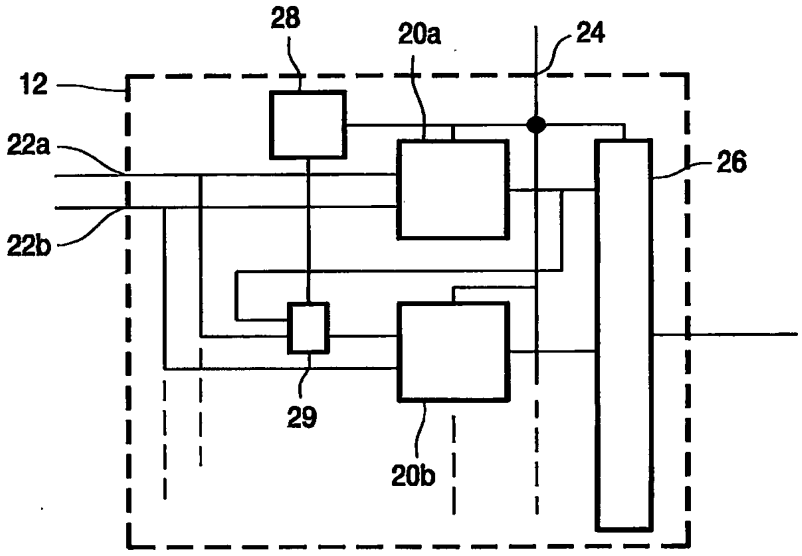

FIG. 2

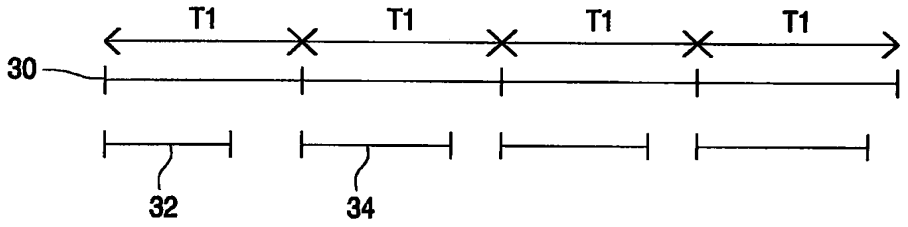

FIG. 3A

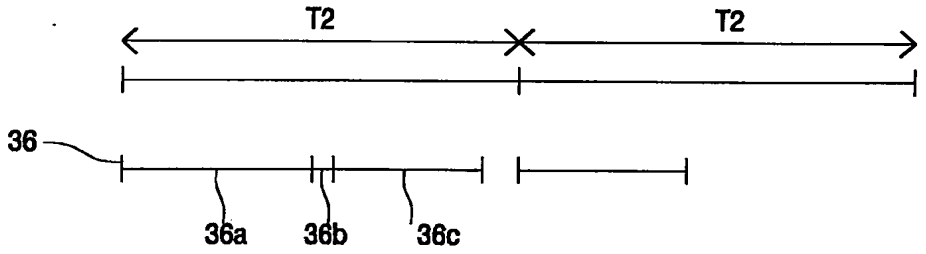

FIG. 3B

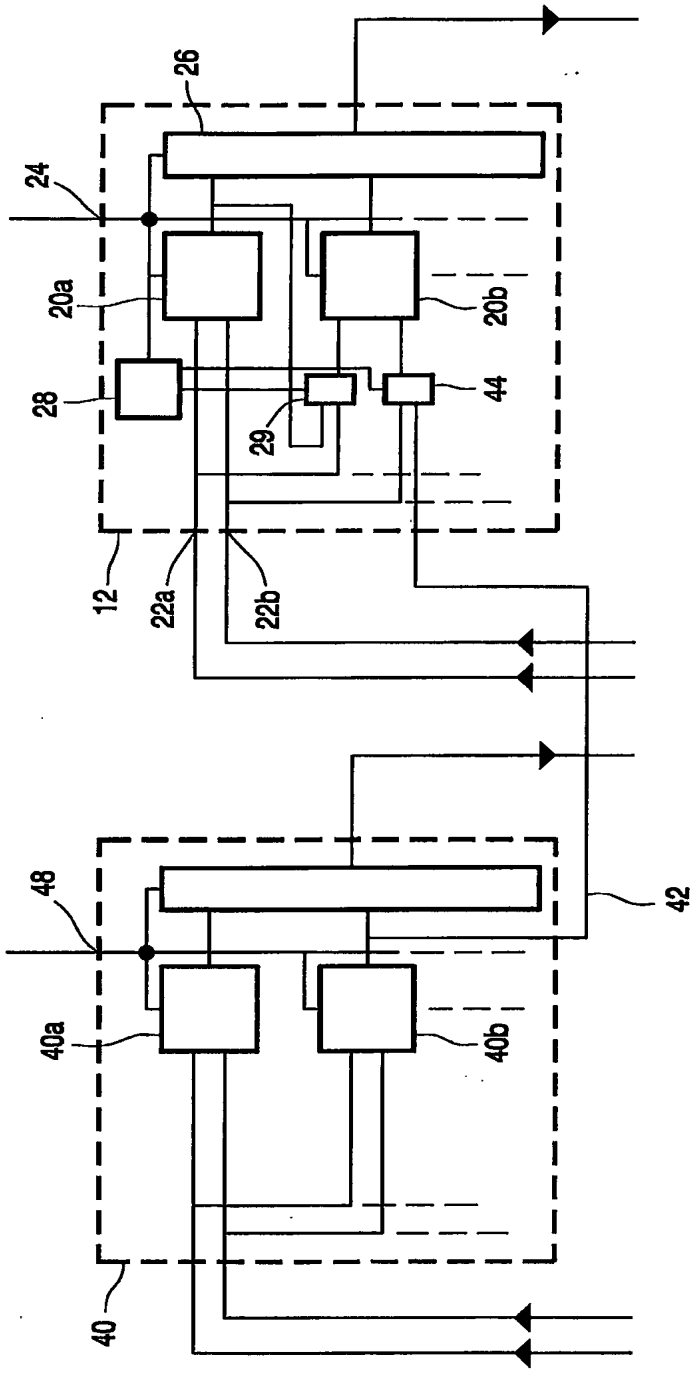

FIG. 4

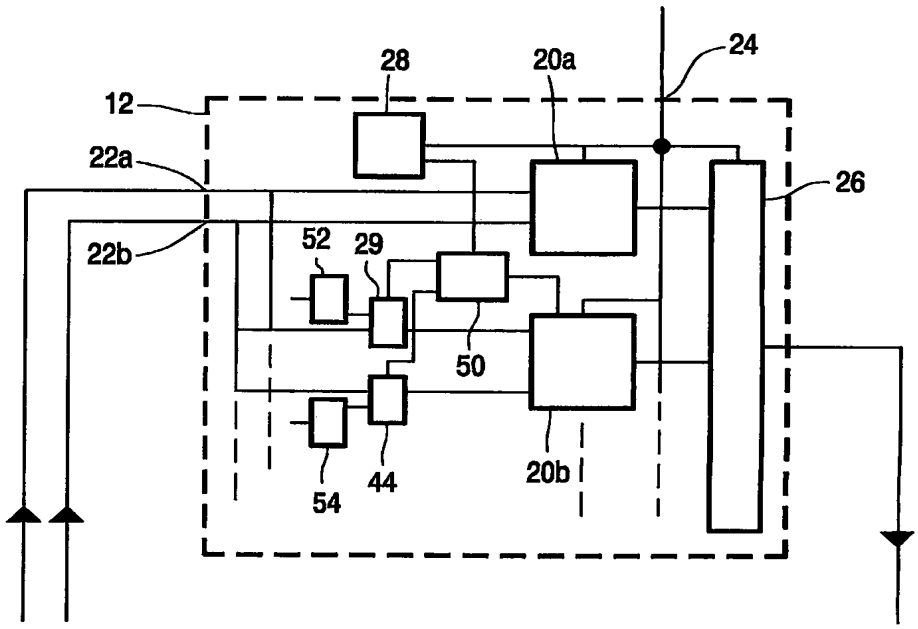

FIG. 5